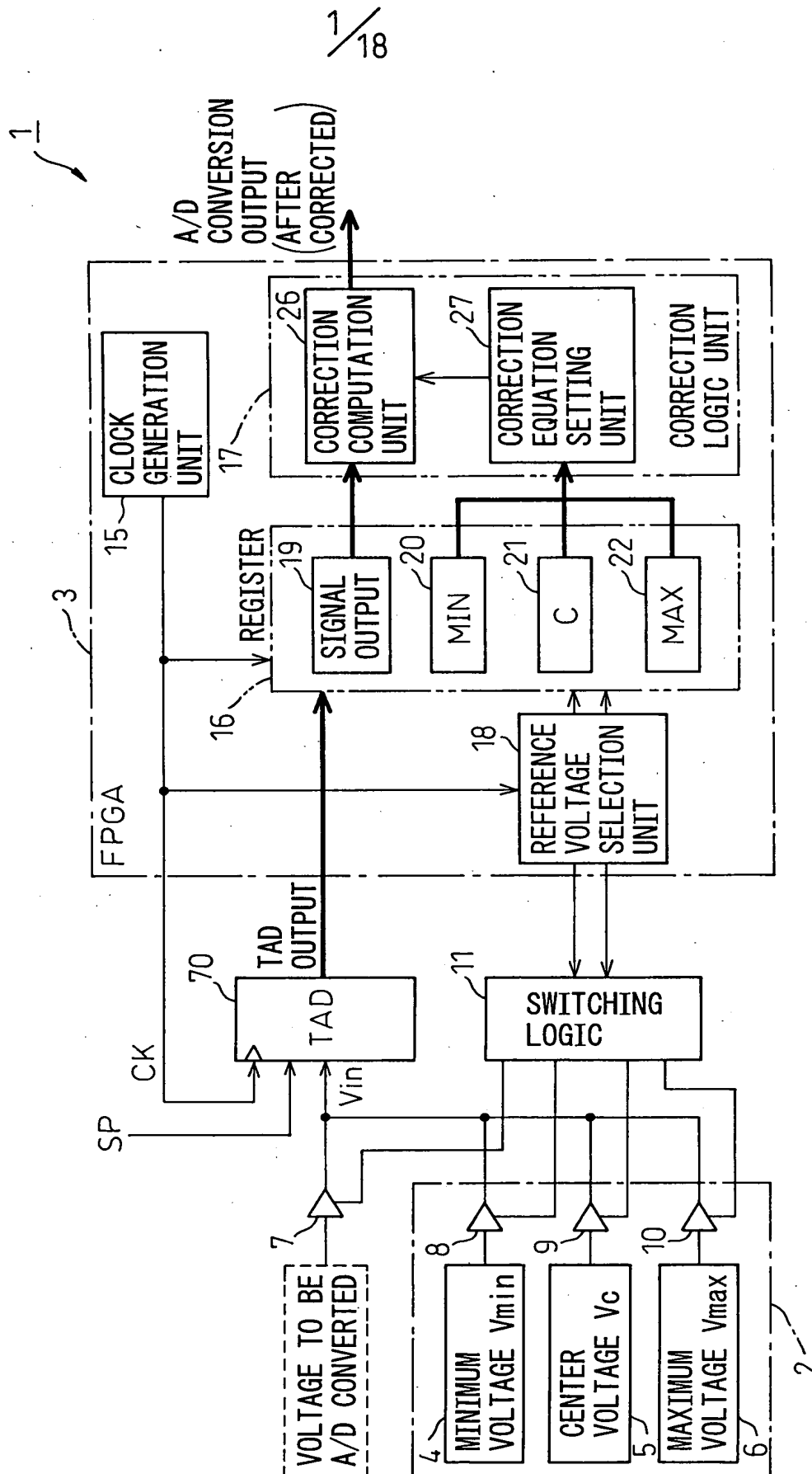


Fig.1



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Fig.2

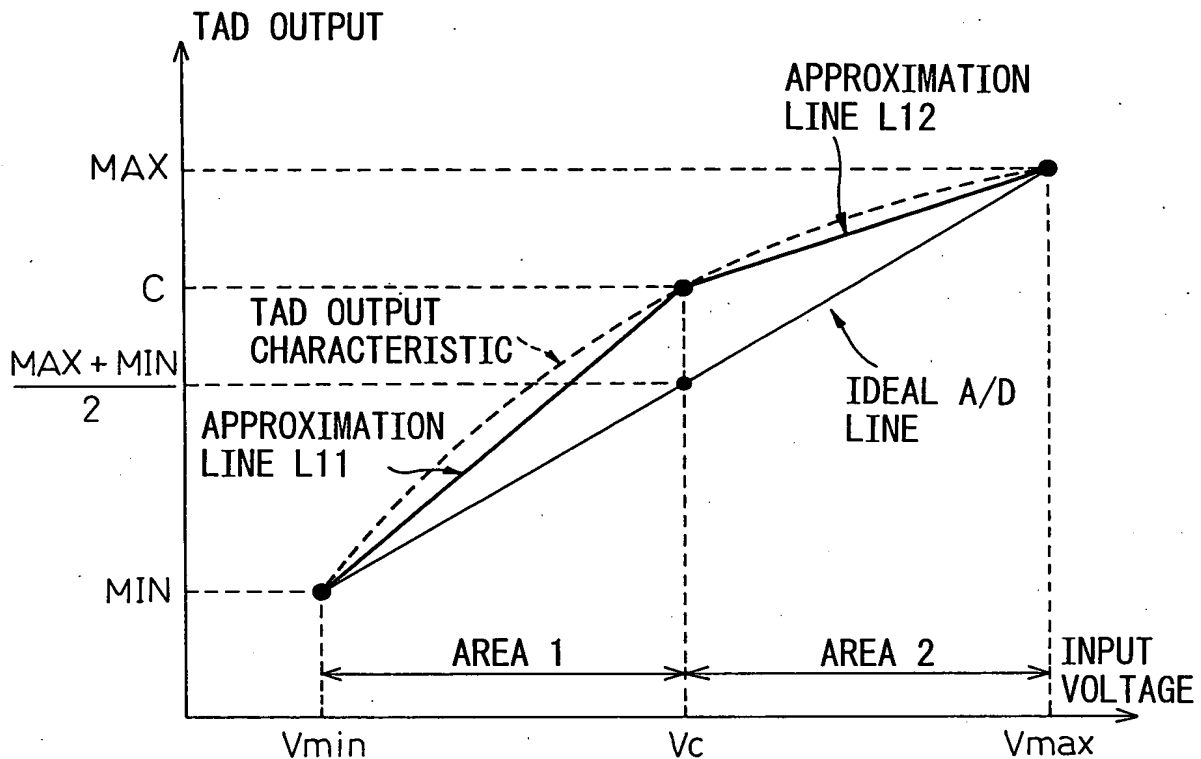
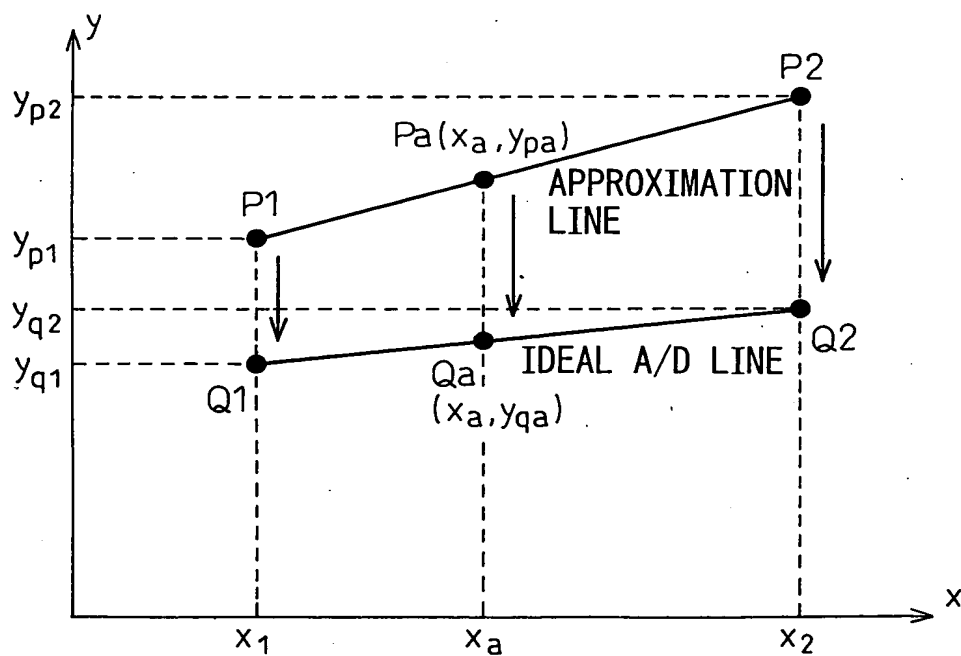
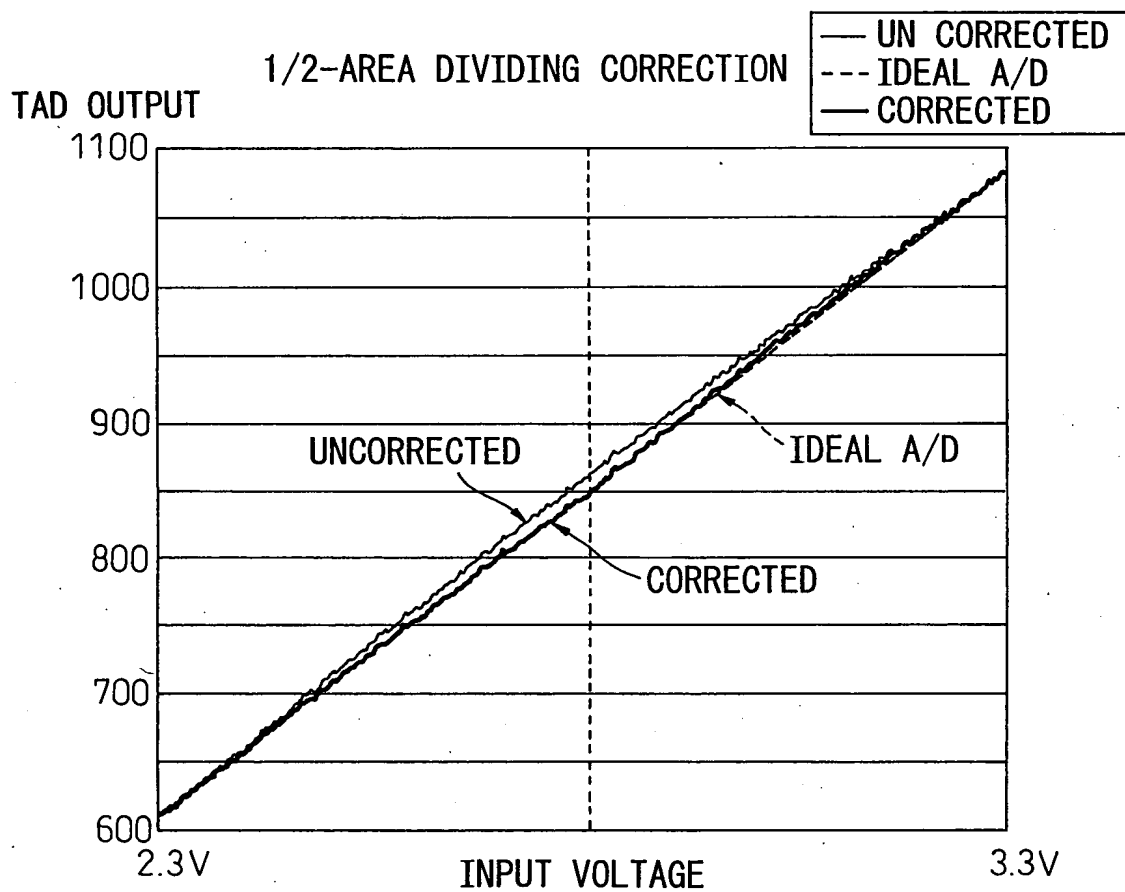


Fig.3



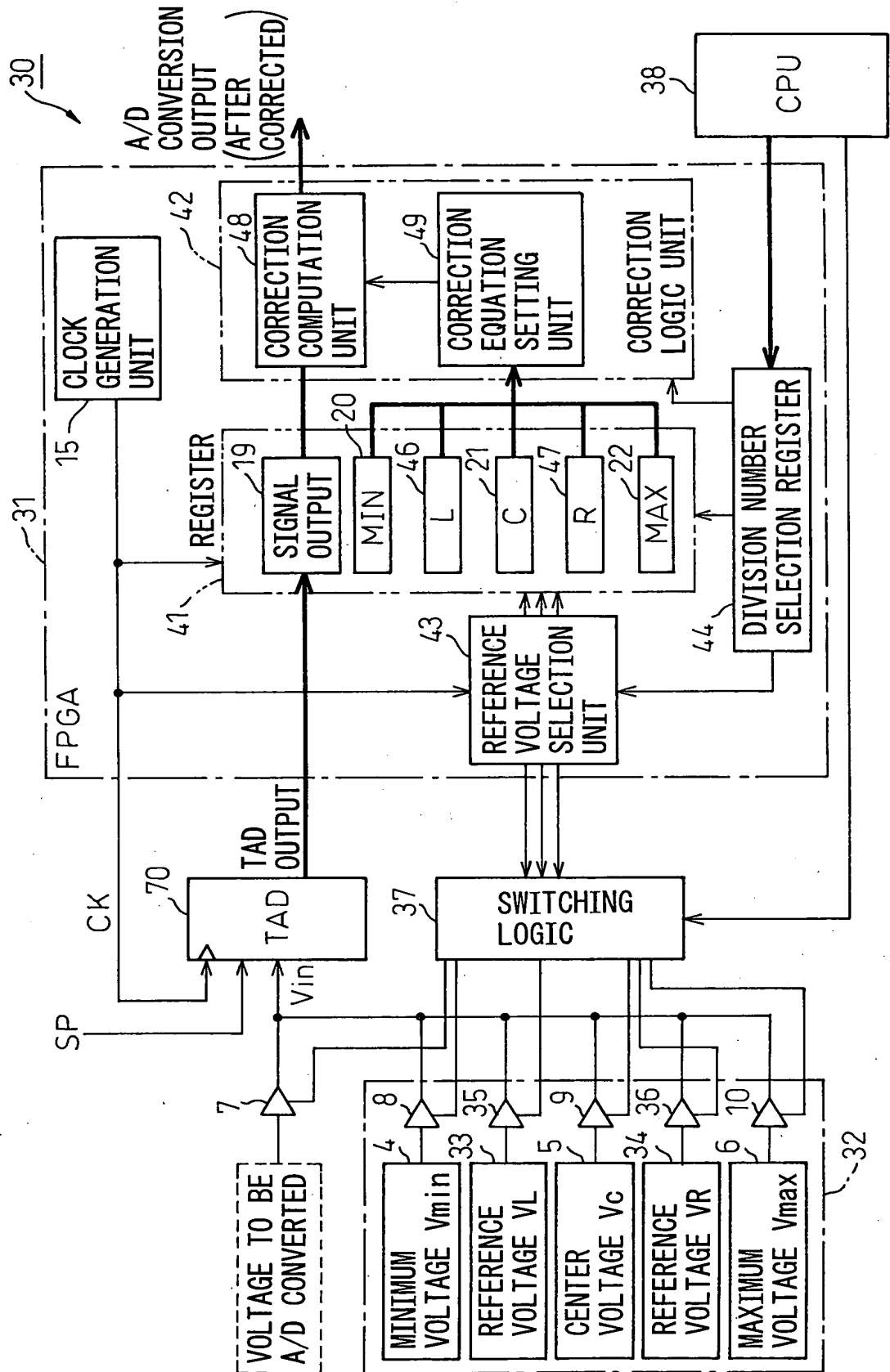
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Fig.4



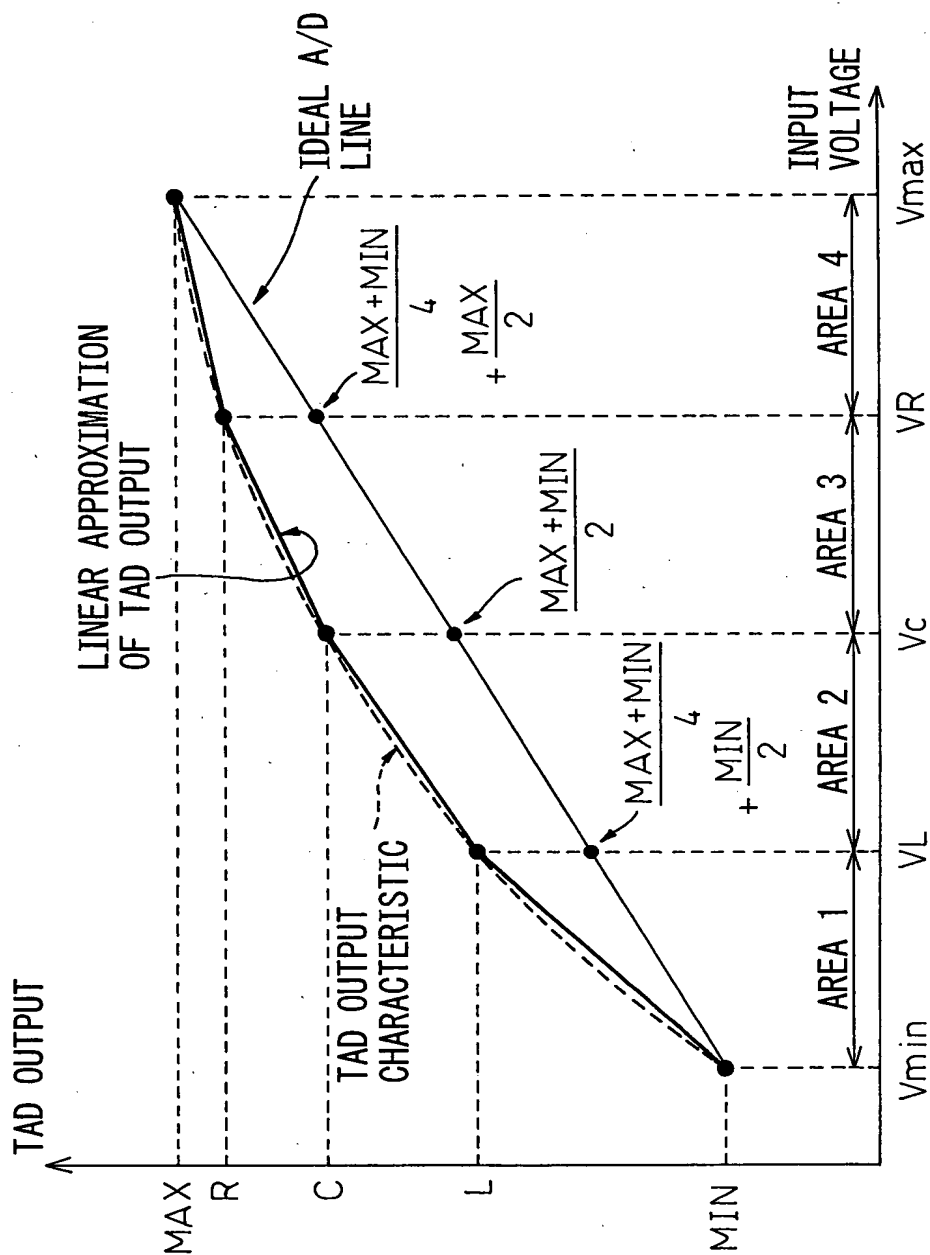
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Fig.5



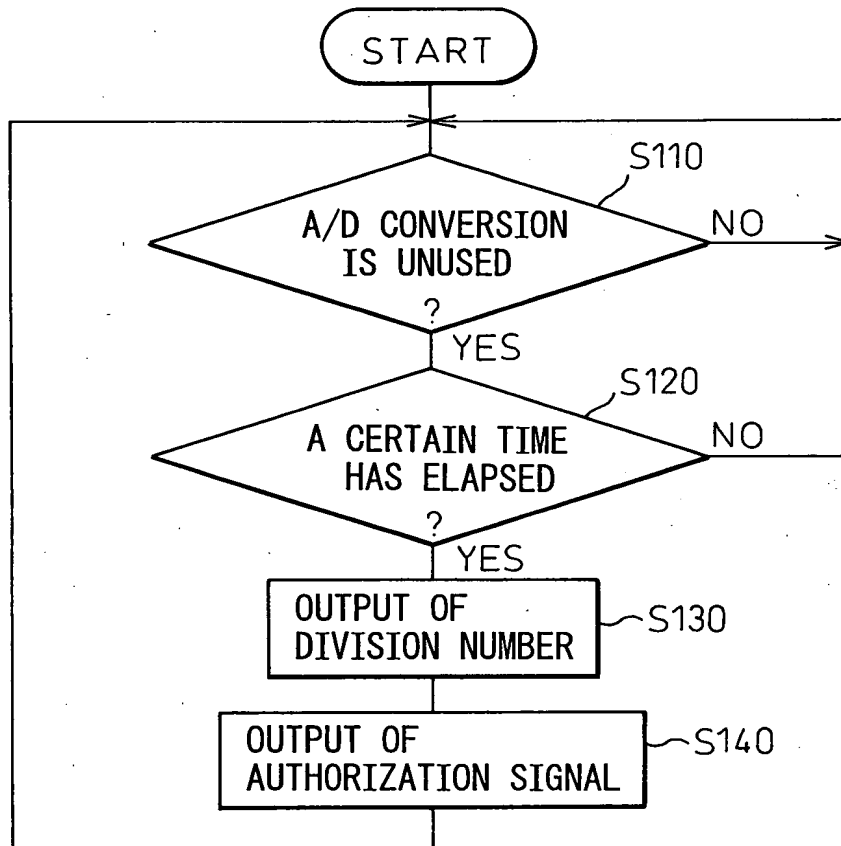
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Fig.6



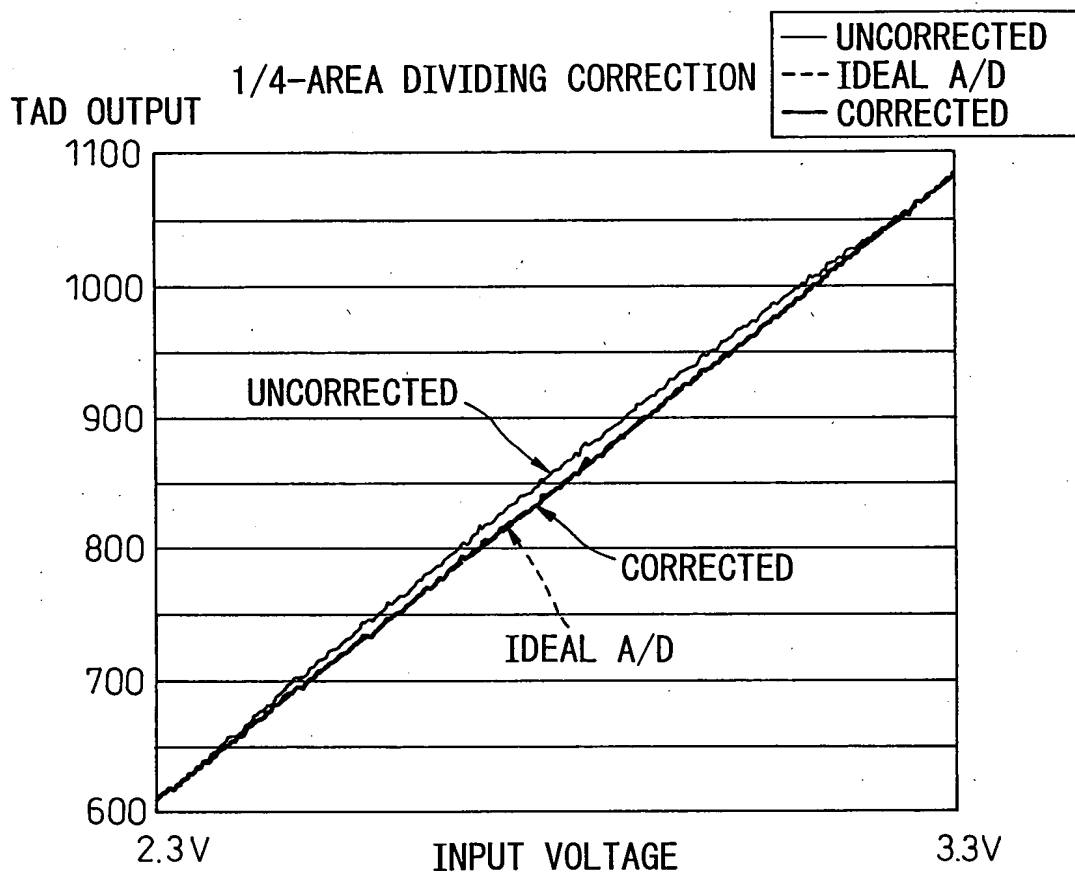
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Fig. 7



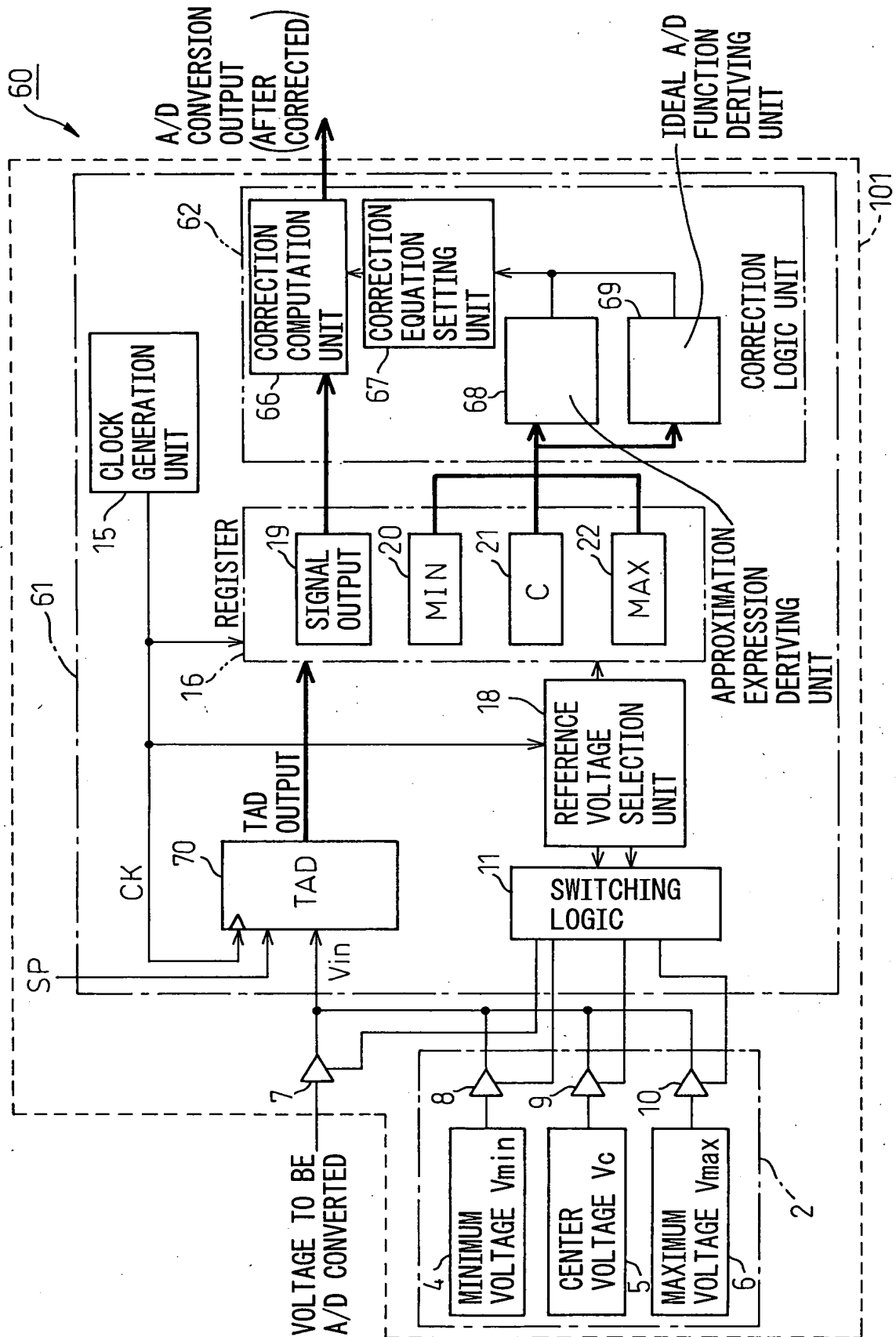
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Fig.8



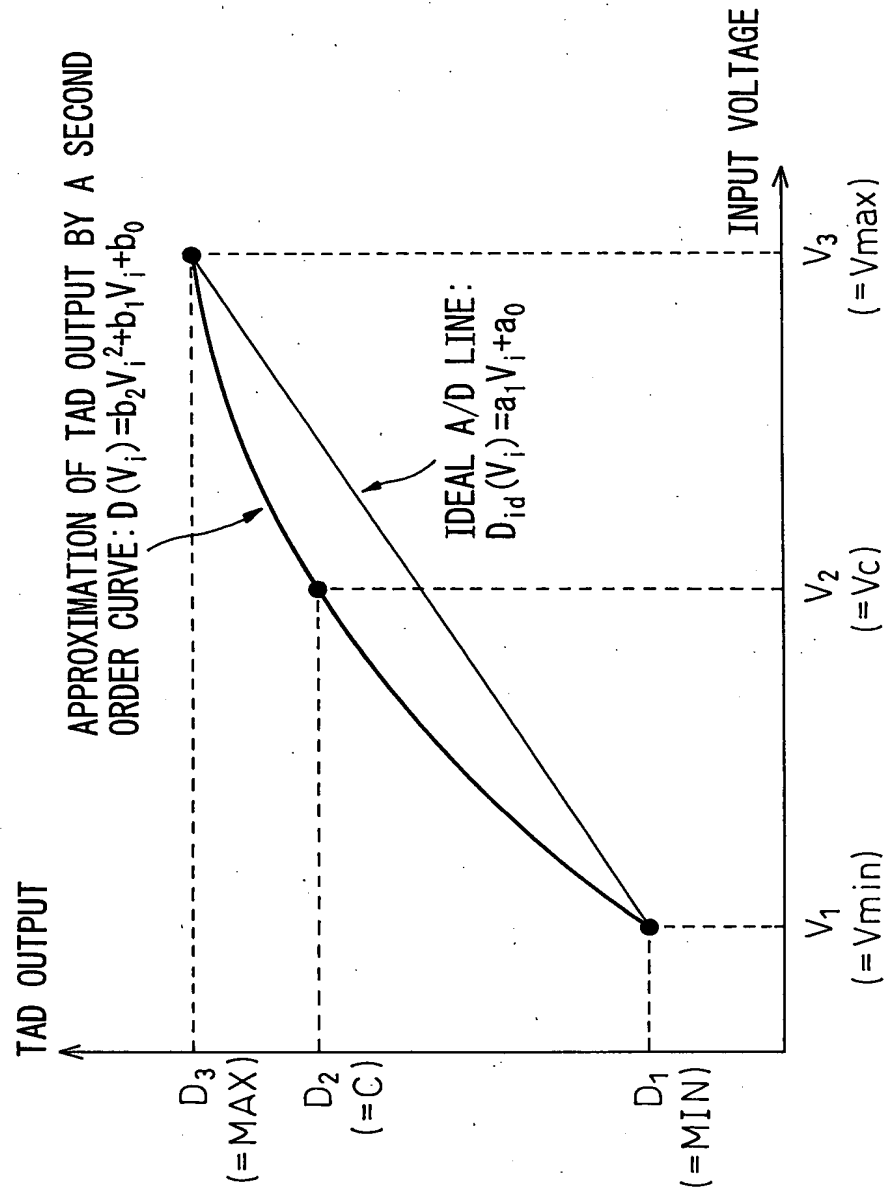
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Fig.9



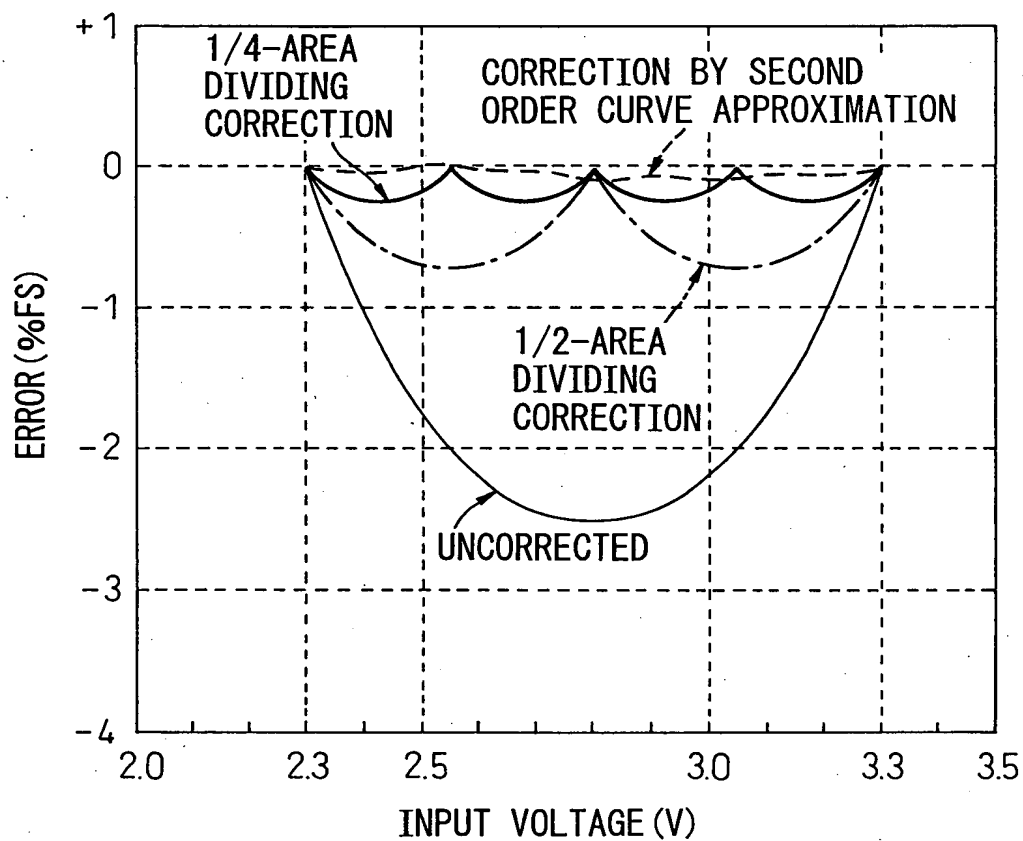
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Fig.10



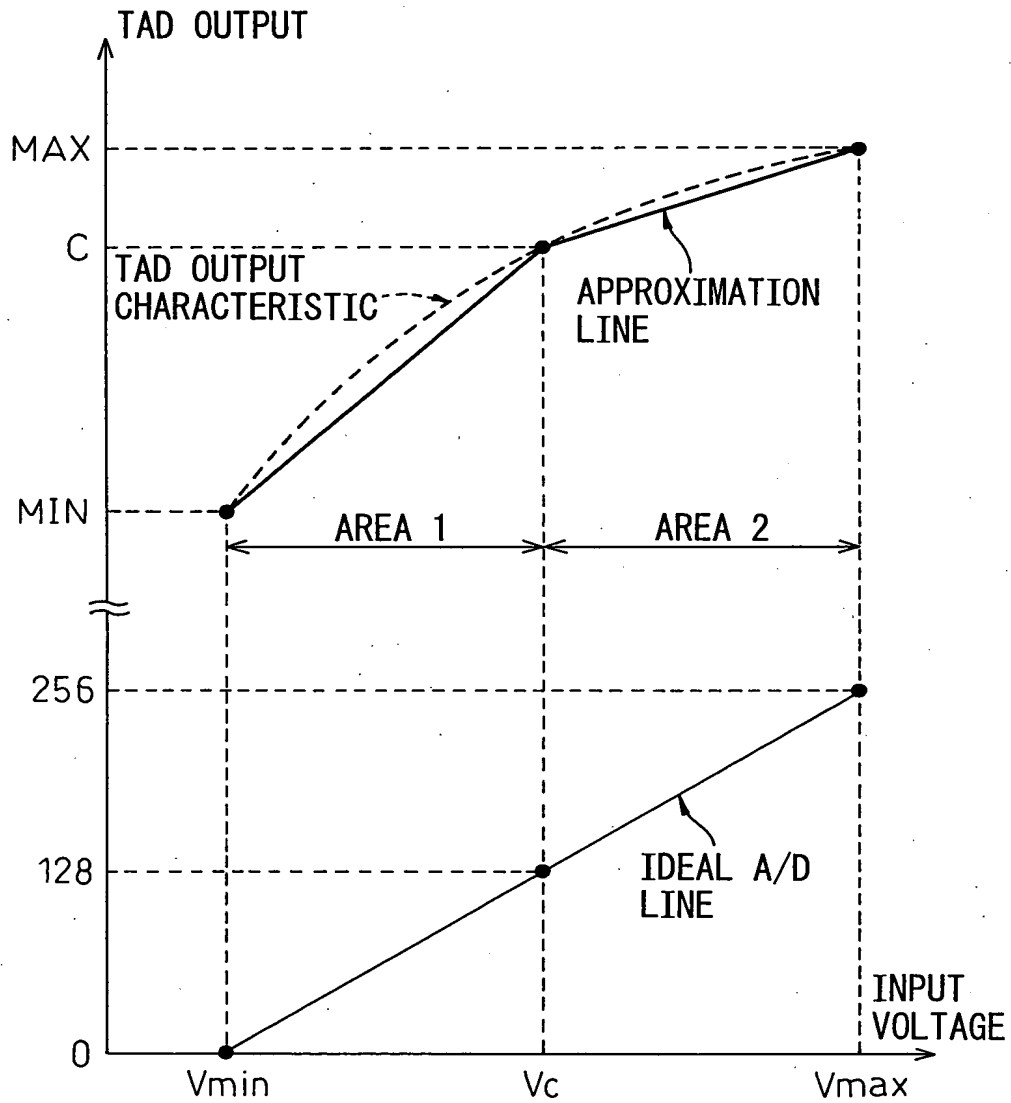
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Fig.11



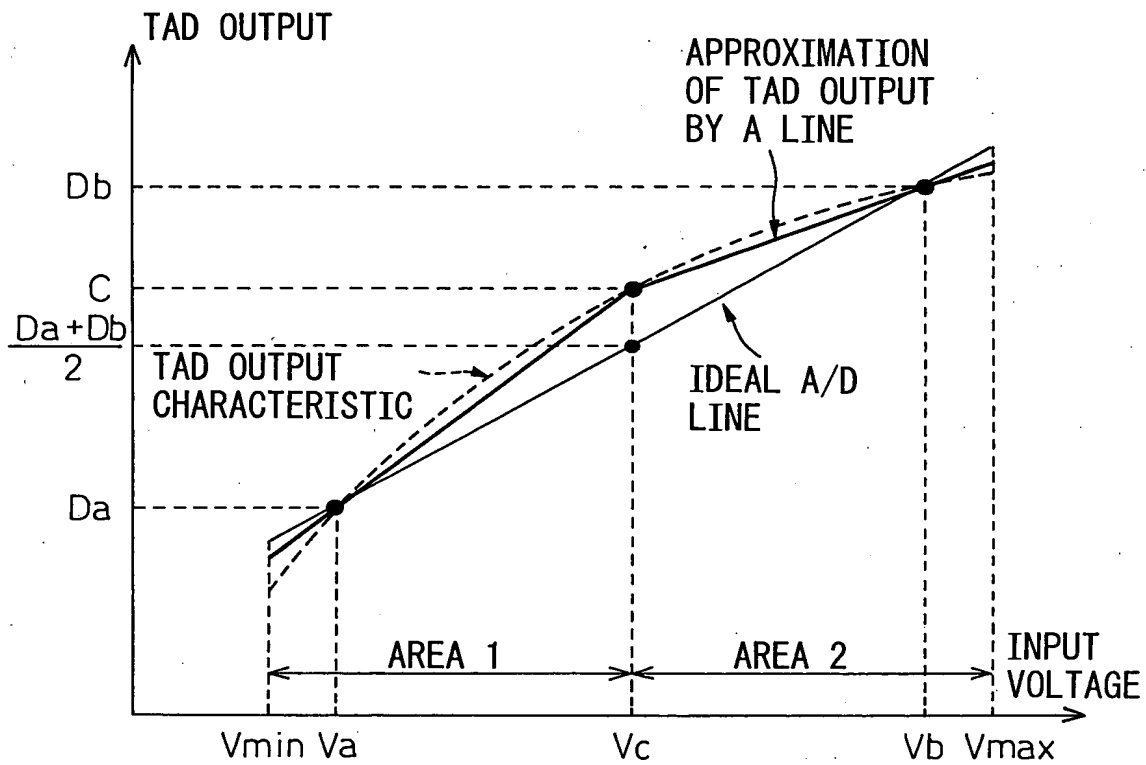
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Fig.12



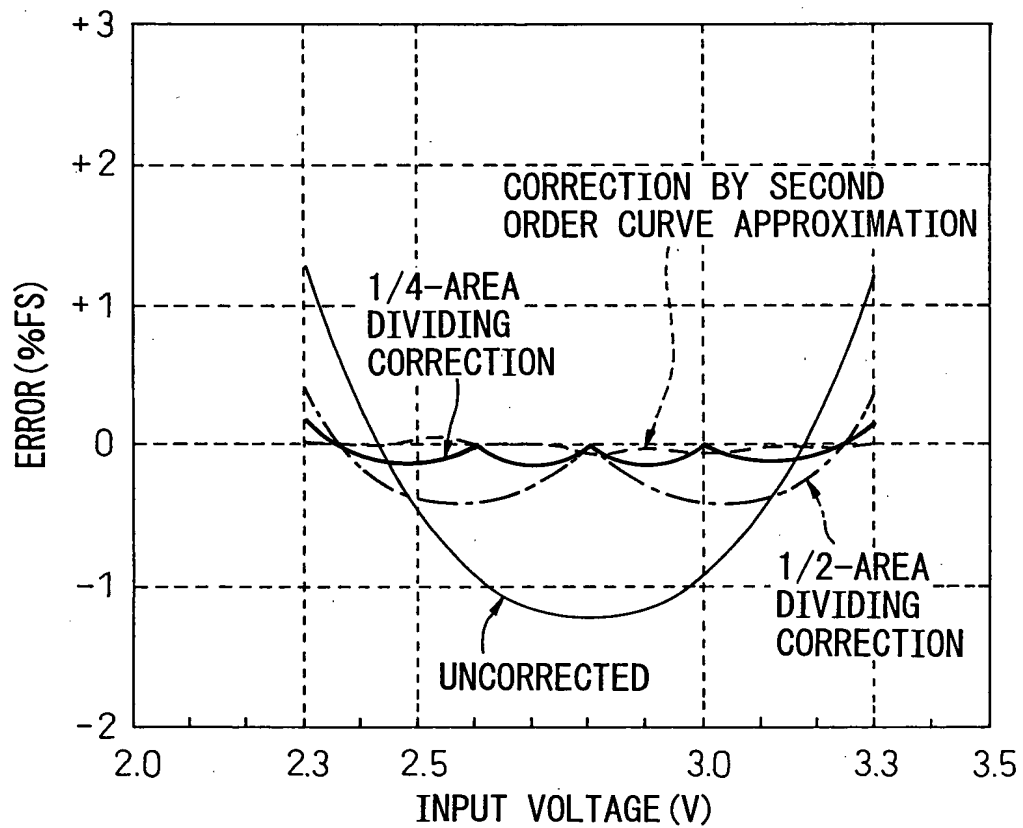
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Fig.13



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Fig.14



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Fig.15

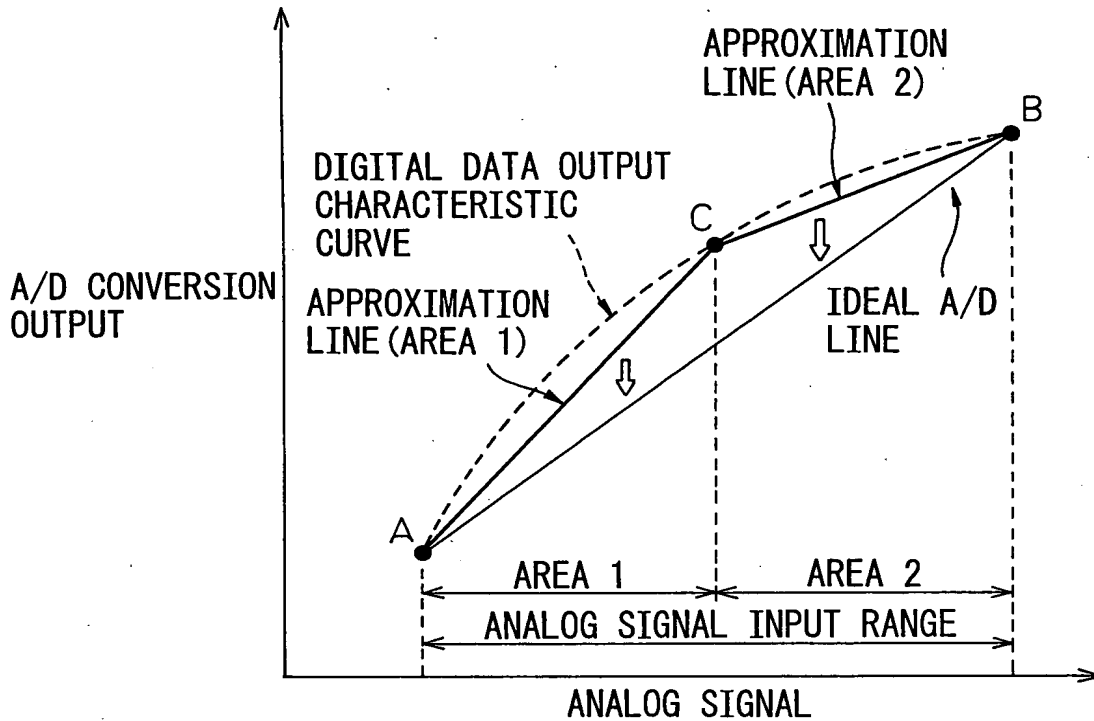
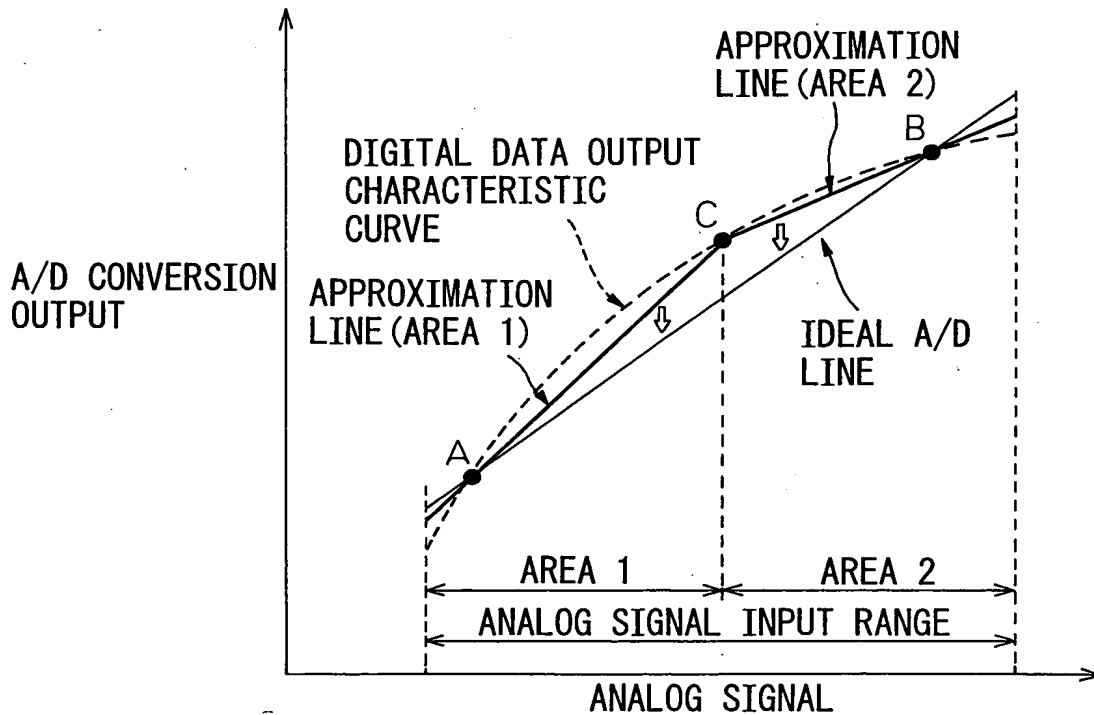


Fig.16



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Fig.17

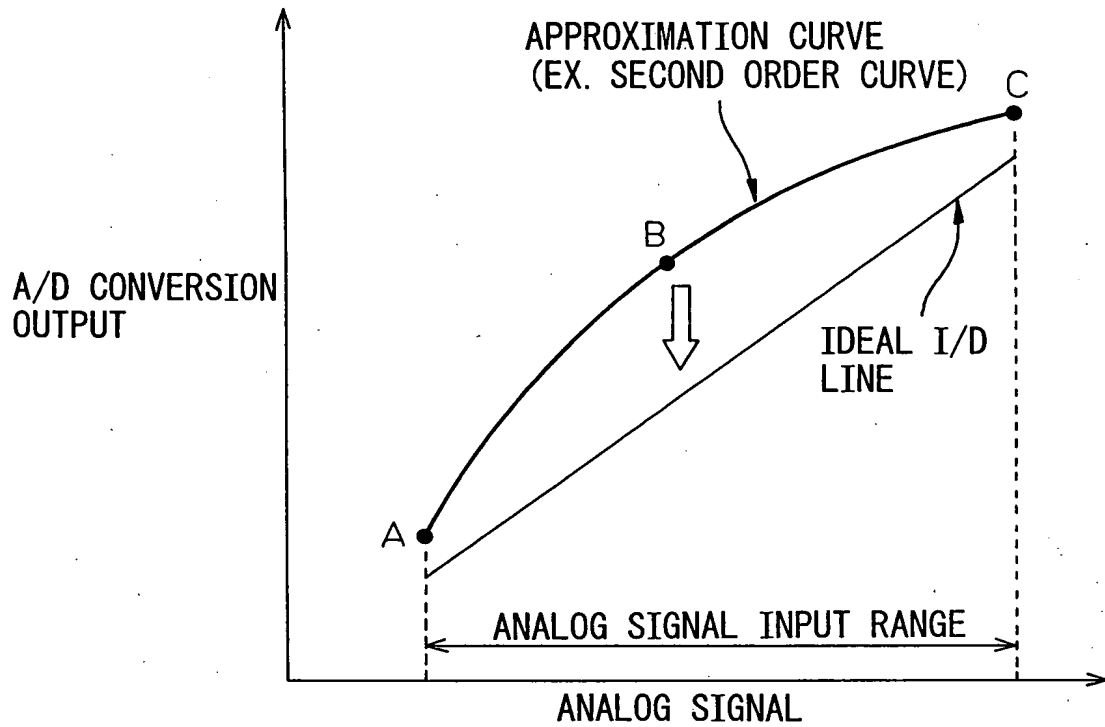
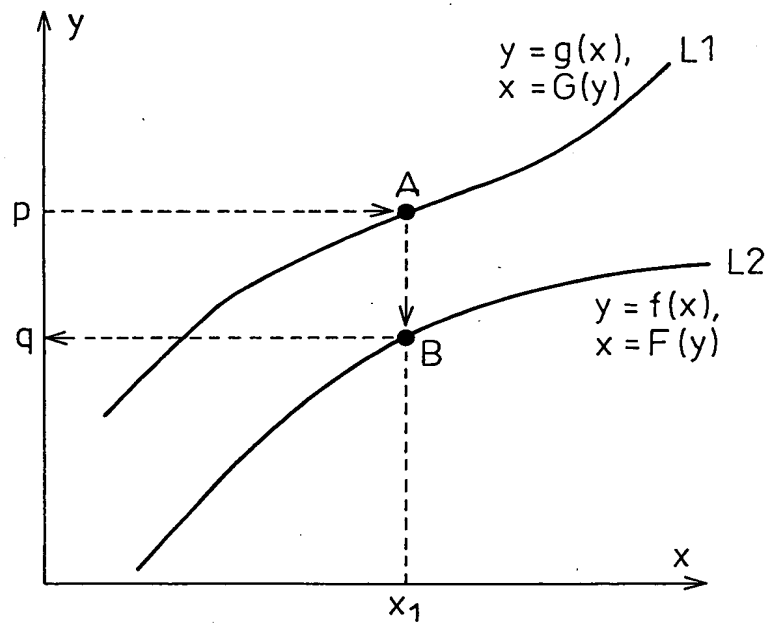
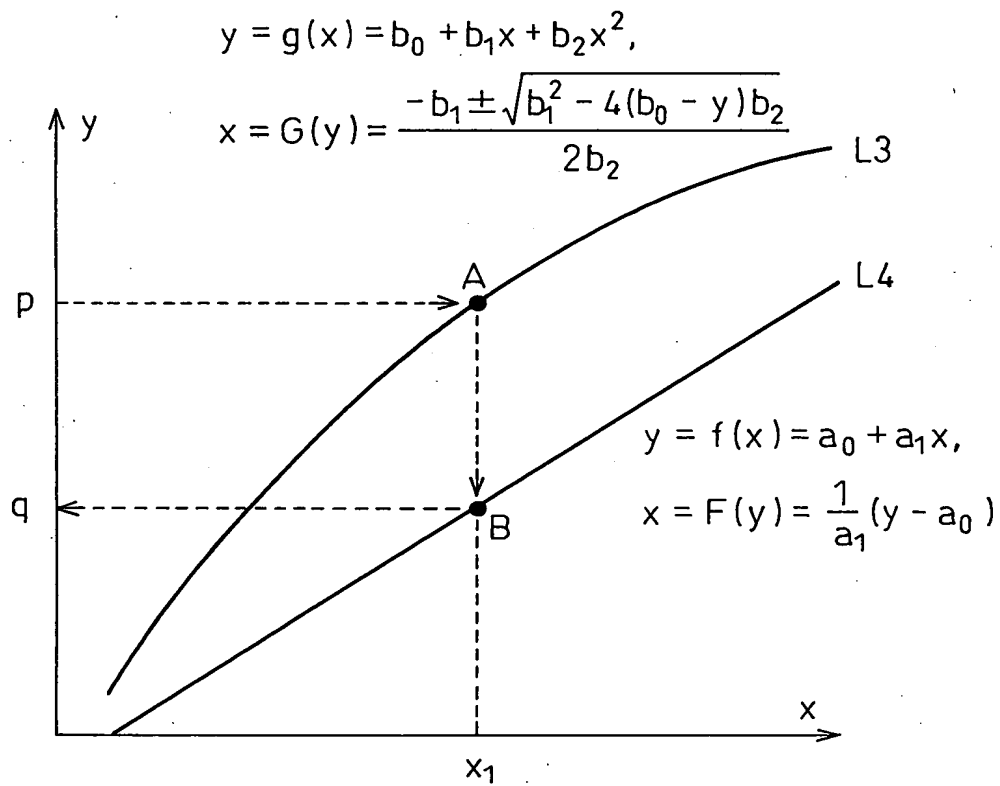


Fig.18



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Fig.19



The diagram illustrates a TAD (Time-to-Digital) converter circuit, labeled 70. The circuit is divided into two main sections: a top section (71) and a bottom section (72). The top section (71) contains a COUNTER (74) and a LATCH (75). The bottom section (72) contains a LATCH & ENCODER (73) and a LATCH (76). The circuit is controlled by three inputs: INPUT VOLTAGE V_{in} , START PULSE SP, and SAMPLING CLOCK CK. The INPUT VOLTAGE V_{in} is connected to the COUNTER (74). The START PULSE SP is connected to the LATCH & ENCODER (73). The SAMPLING CLOCK CK is connected to the LATCH & ENCODER (73) and the LATCH (76). The COUNTER (74) outputs a 14-bit signal to the LATCH (75). The LATCH & ENCODER (73) outputs a 4-bit signal to the LATCH (75). The LATCH (75) outputs an 18-bit signal, labeled DT (18bit), to a summing junction (77). The summing junction (77) also receives a feedback signal from the LATCH (76), labeled DATA AT ONE PREVIOUS SAMPLING CLOCK. The output of the summing junction (77) is the TAD OUTPUT (18bit).

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Fig.21

